

N-Channel Enhancement-Mode MOS Transistors

Product Summary

Part Number	V _{(BR)DSS} Min (V)	r _{D(on)} Max (Ω)	V _{GS(th)} (V)	I _D (A)
VN0808L	80	4 @ V _{GS} = 10 V	0.8 to 2	0.3
VN0808M		4 @ V _{GS} = 10 V	0.8 to 2	0.33
VQ1006P	90	4 @ V _{GS} = 10 V	0.8 to 2.5	0.4

Features

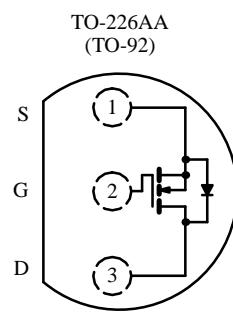
- Low On-Resistance: 3.6 Ω
- Low Threshold: 1.6 V
- Low Input Capacitance: 35 pF
- Fast Switching Speed: 6 ns
- Low Input and Output Leakage

Benefits

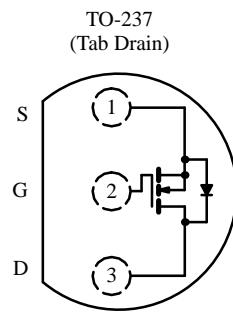
- Low Offset Voltage
- Low-Voltage Operation
- Easily Driven Without Buffer
- High-Speed Circuits
- Low Error Voltage

Applications

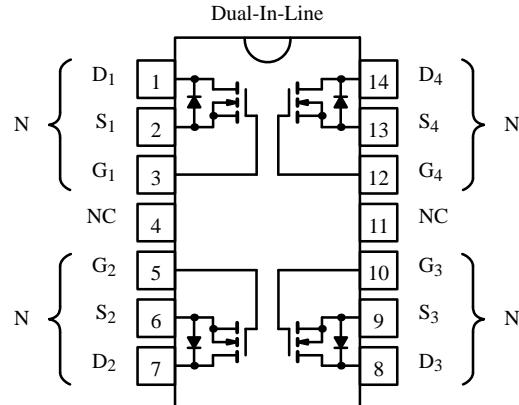
- Direct Logic-Level Interface: TTL/CMOS
- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories, Transistors, etc.
- Battery Operated Systems
- Solid-State Relays



Top View
VN0808L



Top View
VN0808M



Top View
Sidebrazed: VQ1006P

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter	Symbol	VN0808L	VN0808M	VQ1006P		Unit
				Single	Total Quad	
Drain-Source Voltage	V _{DS}	80	80	90		V
Gate-Source Voltage	V _{GS}	±30	±30	±20		
Continuous Drain Current (T _J = 25°C) (T _A = 100°C)	I _D	0.3	0.33	0.4		A
		0.19	0.21	0.23		
Pulsed Drain Current ^a	I _{DM}	1.9	1.9	2		
Power Dissipation (T _A = 25°C) (T _A = 100°C)	P _D	0.8	1	1.3	2	W
		0.32	0.4	0.52	0.8	
Maximum Junction-to-Ambient	R _{thJA}	156	125	96	62.5	°C/W
Operating Junction and Storage Temperature Range	T _J , T _{stg}			−55 to 150		°C

Notes

a. Pulse width limited by maximum junction temperature.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70214.

VN0808L/M, VQ1006P

TEMIC
Semiconductors

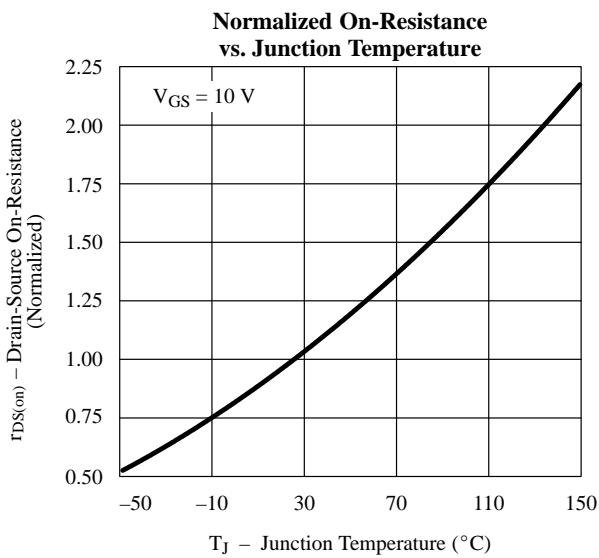
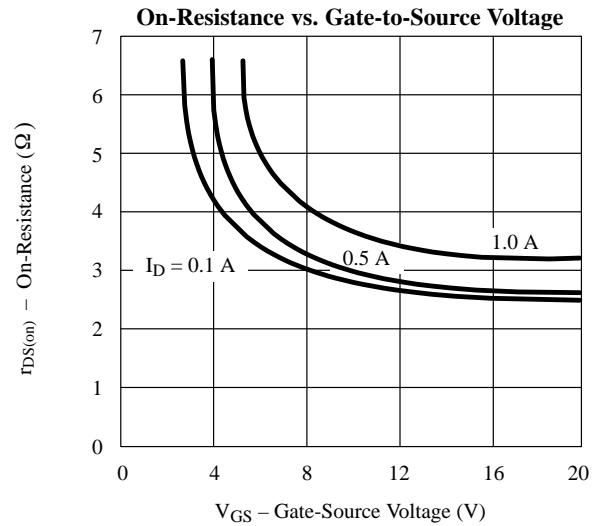
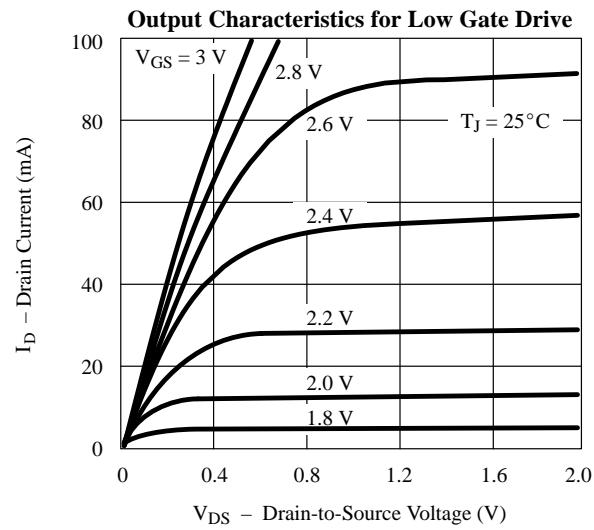
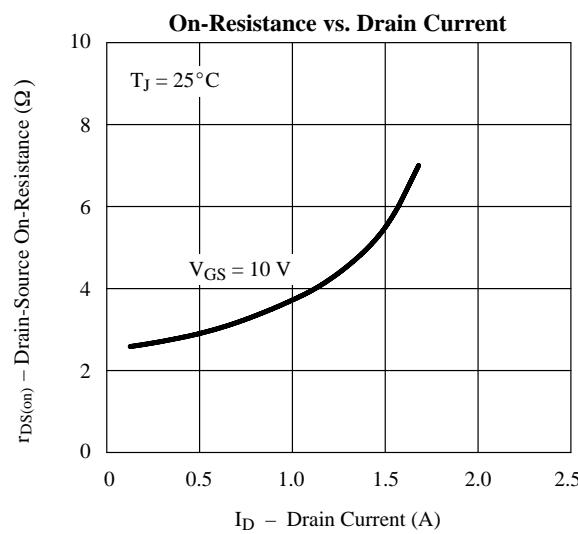
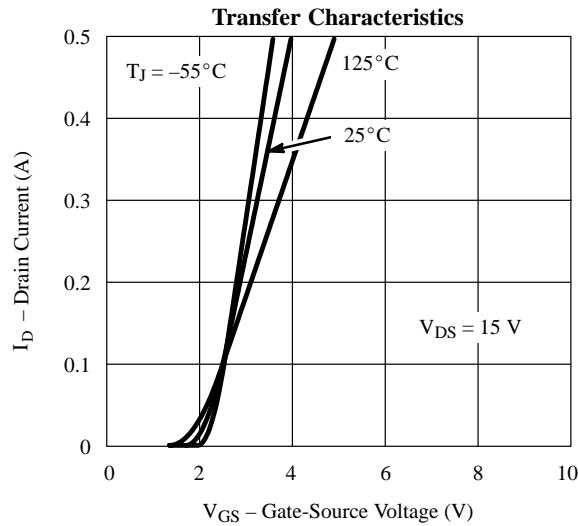
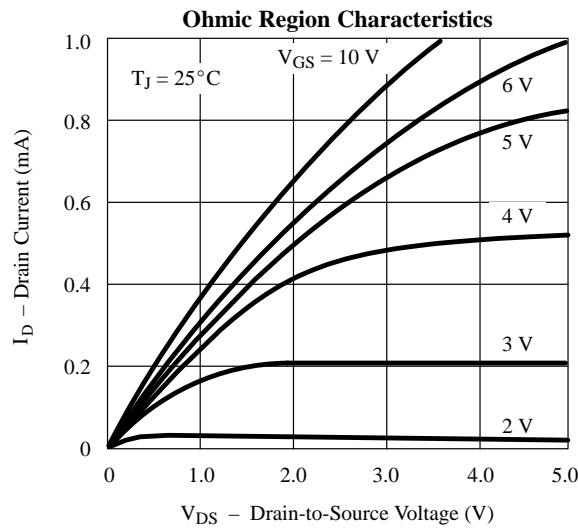
Specifications^a

Parameter	Symbol	Test Conditions	Typ ^b	Limits				Unit	
				VN0808L/M		VQ1006P			
				Min	Max	Min	Max		
Static									
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0 \text{ V}, I_D = 10 \mu\text{A}$	125	80		90		V	
Gate-Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 1 \text{ mA}$	1.6	0.8	2	0.8	2.5		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 15 \text{ V}$ $T_J = 125^\circ\text{C}$			± 100		± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$ $T_J = 125^\circ\text{C}$			10			μA	
		$V_{DS} = 72 \text{ V}, V_{GS} = 0 \text{ V}$ $T_J = 125^\circ\text{C}$			500				
						1			
On-State Drain Current ^c	$I_{D(\text{on})}$	$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}$	1.8	1.5		1.5		A	
Drain-Source On-Resistance ^c	$r_{DS(\text{on})}$	$V_{GS} = 5 \text{ V}, I_D = 0.3 \text{ A}$	3.8			5		Ω	
		$V_{GS} = 10 \text{ V}, I_D = 1 \text{ A}$ $T_J = 125^\circ\text{C}$	3.6		4		4.5		
			6.7		8		8.6		
Forward Transconductance ^c	g_{fs}	$V_{DS} = 10 \text{ V}, I_D = 0.5 \text{ A}$	350	170		170		mS	
Common Source Output Conductance ^c	g_{os}	$V_{DS} = 10 \text{ V}, I_D = 0.1 \text{ A}$	0.23						
Dynamic									
Input Capacitance	C_{iss}	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	35		50		60	pF	
Output Capacitance	C_{oss}		15		40		50		
Reverse Transfer Capacitance	C_{rss}		2		10		10		
Switching^d									
Turn-On Time	t_{ON}	$V_{DD} = 25 \text{ V}, R_L = 23 \Omega$ $I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}$ $R_G = 25 \Omega$	6		10		10	ns	
Turn-Off Time	t_{OFF}		8		10		10		

Notes

- a. $T_A = 25^\circ\text{C}$ unless otherwise noted.
- b. For DESIGN AID ONLY, not subject to production testing.
- c. Pulse test: $PW \leq 300 \mu\text{s}$ duty cycle $\leq 2\%$.
- d. Switching time is essentially independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted) (Cont'd)

